A 44-GHz High IP3 InP-HBT Amplifier with Practical Current Reuse Biasing

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***Abstract*—This paper will discuss the practical design of an InP-based heterojunction bipolar transistor (HBT) Q-band high IP3 monolithic microwave integrated circuit (MMIC) amplifier. The amplifier features a novel "double-balanced" design approach that incorporates a practical "current reuse" biasing scheme. The current reuse biasing results in a 40% reduction in current consumption through a standard 5-V supply and simplifies the MMIC's system integration while the double-balanced design produces wide-band IP3, gain, and excellent out-of-band return-loss performance required for practical applications. The three-stage MMIC amplifier achieves 15.4 dB of gain, 28.3 dBm of IP3, and a P_{sat} of 16.2 dBm at 44 GHz. An output-stage IP3/P_{dc} ratio linearity-figure-of-merit of 5.3 is obtained and is believed to be among the best reported for an InP-HBT amplifier operating at Q-band frequencies. The IP3 performance was optimized using load–pull simulations based on a custom HBT IP3 model. Different device cell configurations such as the common-emitter, common-base, and cascode were also considered. The common-emitter amplifier results of this paper demonstrate the promising linearity performance of InP-HBT's and its practical bias and integration capability which is attractive for Q-band receiver applications.**

***Index Terms*— HBT, InP, IP3, linearity, millimeter-wave, MMIC amplifier.**

I. Introduction

HIGH IP3 amplifiers are needed in millimeter-wave receiver systems such as Ka- and Q-band digital radio applications. For frequencies below 18 GHz, GaAs heterojunction bipolar transistors (HBT's) [1] as well as spiked and pulsed-doped MESFET's [2], [3] have demonstrated record circuit linearity figure of merits (LFOM = IP3/$P_{\rm dc}$) which are an order of magnitude better than conventional MESFET amplifiers. However, for the millimeter-wave regime, little has been published on the circuit linearity merits of these technologies due to their modest frequency and gain performance. For practical millimeter-wave applications there are more design considerations such as gain or number of gain stages, bandwidth performance, and practical on-chip bias implementation. For example, having wide-band gain, IP3, and excellent return-loss performance can minimize the amplifier's performance degradation when it is inserted into a system with other components such as a mixer and voltage-controlled oscillator (VCO), even when the application only requires a narrow operating bandwidth. In addition to the desensitized insertion performance, it is also desirable to employ monolithic self-bias which can result in a significant reduction in size and part count by eliminating the discrete off-chip bias regulators which are often required to accommodate the lower monolitic microwave integrated circuit (MMIC) supply voltages of 2–3 V. The reduced millimeter-wave assembly size has the added benefit of minimizing the chance of cavity mode effects as well. At millimeter-wave frequencies, HBT technology can provide high performance and facilitate practical system insertion.

Recently, a GaAs/AlGaAs HBT amplifier was reported which achieved an IP3 of 24–30 dBm and an LFOM of 3–11.6 in a band from 38–44 GHz [4]. An InP-HBT amplifier has also been reported which achieved an IP3 of 26.5 dBm and an LFOM of 4.1 at 35 GHz [5]. InP-based HBT's, while not as mature as GaAs HBT's, can ultimately provide higher gain and frequency performance for less dc power consumption due to their higher peak electron velocity and lower voltage (bandgap) operation [6]. Furthermore, their lower V_{ce} operation is better suited for "current reuse" biasing techniques in which the transistors of different amplifier stages share the same current through a dc totem-pole or stacked device configuration with a standard fixed supply voltage such as 5 V.

In this paper, we describe the design and IP3 performance of a Q-band InP-HBT MMIC amplifier which features a double-balanced amplifier topology that incorporates a practical current reuse self-bias scheme. The following sections will describe the MMIC amplifier technology and design. In particular, Section II will cover device technology and suitability to low voltage and millimeter-wave amplifier applications, Section III will describe the design motivation and requirements, Sections IV and V discuss the HBT IP3 modeling and circuit design, and Section VI reveals the measured performance of the fabricated InP-HBT Q-band amplifier.

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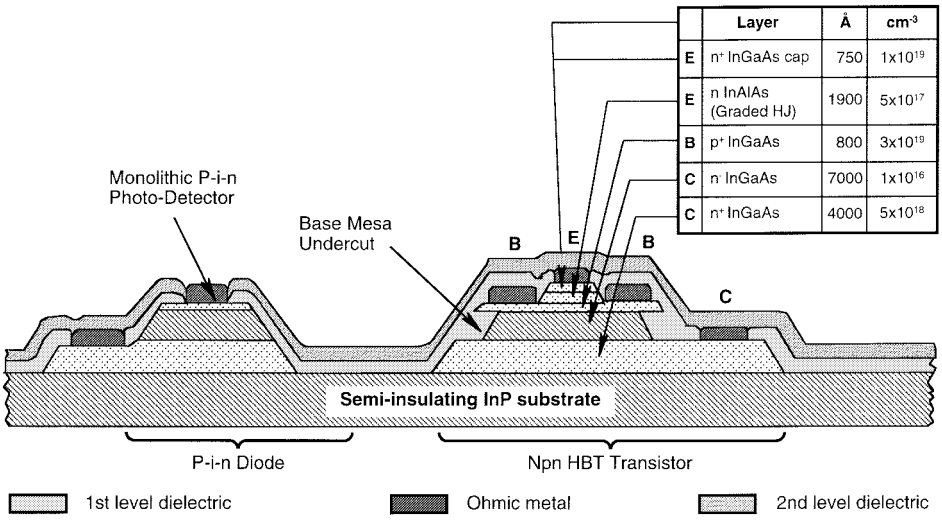
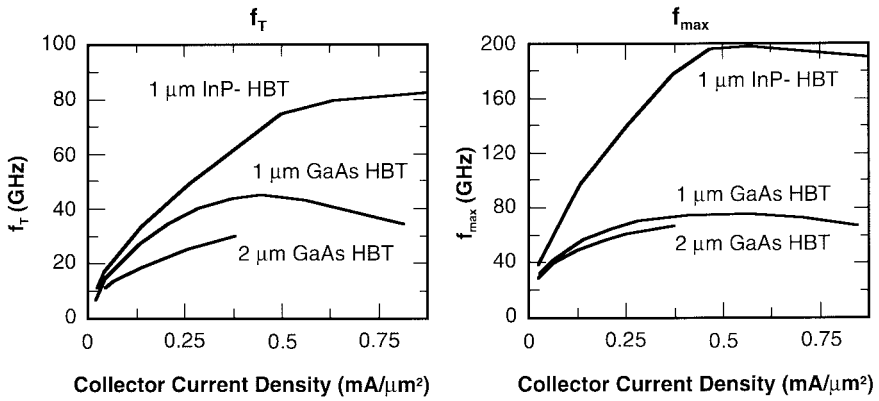


Fig. 1. Cross section of TRW's InAlAs/InGaAs–InP HBT device technology.



(a) (b)

Fig. 2. Comparison of HBT (a) f_T and (b) $f_{\max}$ capability for both AlGaAs/GaAs and InAlAs/InGaAs–InP HBT device technologies.

II. InAlAs/InGaAs-InP HBT Device Technology

The Q-band MMIC amplifier reported in this paper is based on an InAlAs/InGaAs–InP HBT device technology. Fig. 1 shows a cross section of TRW's InAlAs/InGaAs HBT device structure. The InAlAs/InGaAs HBT device epitaxy is grown by molecular beam epitaxy (MBE) on a 3-in semi-insulating InP substrate. Be and Si are used as p- and n-type dopants for the base and emitter/collector, respectively. The emitter incorporates a 750-Å InGaAs cap which is highly doped to obtain low emitter contact resistance. The intrinsic emitter region is 1900 Å thick and doped to 5×10^{17} cm^{-3}. The base-emitter junction is compositionally graded from InGaAs to InAlAs to form HBT's with very repeatable beta and low V_{be} characteristics. The base-collector epitaxial structure consists of a base thickness of 800 Å uniformly doped to 3×10^{19} cm^{-3}, a 7000-Å thick n-type collector lightly doped to 1×10^{16} cm^{-3}, and an n^+ subcollector doped to 5×10^{18} cm^{-3}. The HBT dc beta across the wafers are typically >25–35 at a current density of $J_c = 40$ kA/cm^2. The breakdown voltage BV_{ceo} is ≈8 V, and the BV_{cbo} is ≈13 V which is more than adequate for most RF applications.

A fully self-aligned HBT process is used to produce 1-μm emitter-width HBT's. The HBT's also feature a base-mesa undercut profile that enables a 30–40% reduction in C_{cb} capacitance and results in improved device f_T and $f_{\max}$, as well as millimeter-wave circuit performance [6], [7]. The 1-μm emitter width base-undercut HBT's used in the amplifier design of this work have peak f_T's and $f_{\max}$'s of 75 and 200 GHz (from unilateral gain), respectively. These numbers were achieved from a 1×10 μm^2 quad-emitter HBT biased at a current density of $J_c \approx 40$–50 kA/cm^2 and a $V_{ce} = 2.0$ V.

One key feature of InP-based HBT's which makes them attractive for millimeter-wave applications is that their peak electron velocities are higher than GaAs-based HBT's. Fig. 2 shows a comparison in device f_T and $f_{\max}$ capability for both AlGaAs/GaAs and InAlAs/InGaAs–InP HBT's. While appreciable performance can be obtained by scaling the device geometry as illustrated by the 2- and 1-μm emitter-width GaAs HBT cases, a more dramatic performance improvement is observed when employing the higher speed InP-based HBT's.

However, an even more profound advantage of InP- versus GaAs-HBT's is its low dc voltage operation. Low device

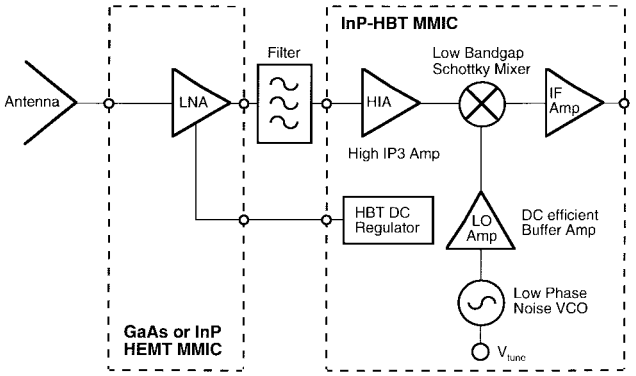


Fig. 3. Block diagram of a typical 44-GHz integrated receiver and the preferred component technology partition.

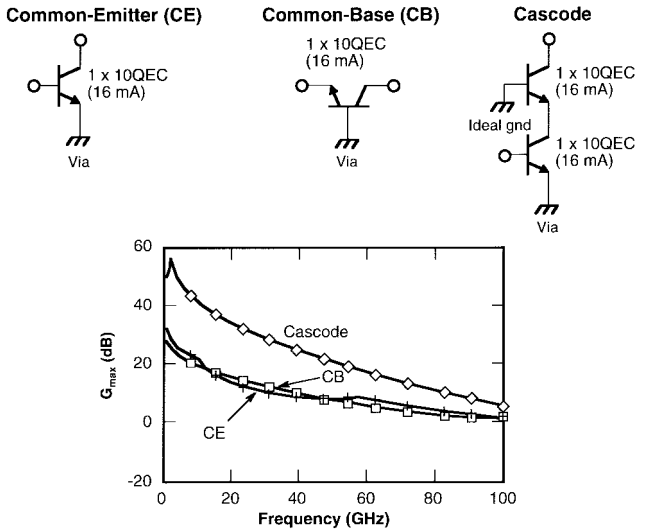


Fig. 4. Comparison of the $G_{\max}$ characteristics of the common-emitter, common-base, and cascode device configurations based on the 1×10 μm^2 quad-emitter HBT unit cell (1×10 QE), biased at an $I_{ce} = 16$ mA and a $V_{ce} = 2.5$ V.

voltage operation is imperative to the "current share" bias approach of this paper and is particularly attractive in space and satellite systems where minimizing the number of voltage regulation tiers results in a savings in dc power, size, weight, and cost. In particular, the low base-emitter turn-on voltage of InAlAs/InGaAs–InP HBT's which is 0.4–0.6 V is about half that of AlGaAs/GaAs HBT's which is in the range of 1.1–1.3 V. In fact, it is even lower than conventional silicon bipolar junction transistors (BJT's), which is around 0.7–0.8 V. This is due in part to the lower intrinsic bandgap of the InGaAs base material as well as the gradual compositional grading of the base-emitter heterojunction commonly employed in III–V semiconductor HBT's. By using low V_{be} turn-on voltage technology such as InP-HBT's, the design robustness of self-bias circuits operating from low supply voltages can be improved. However, it is not only this low turn-on voltage which allows lower operating power, but also the higher peak electron velocity of InGaAs/InP at low electric fields compared to GaAs which enables higher device frequency performance under very low V_{ce} voltage operation. For example, HBT device f_T's of $>$30 GHz can be maintained at a low V_{ce} operating voltage of 0.5 V and a low current density of 25 kA/cm^2. A direct consequence of both these characteristics is that InP-based HBT's have demonstrated the highest amplifier gain-bandwidth product per dc power ratios for supply voltages below 3 V as compared with other technologies [6]. Furthermore, these inherent properties enable them to achieve high performance while conservatively employing relaxed and highly reproducible 1-μm emitter-width process lithography amenable to large scale millimeter-wave commercial production.

III. Design Background and Requirements

A. The Design Motivation

The objective of this paper was to develop a 44-GHz high intercept amplifier based on InP-HBT technology for a millimeter-wave receiver application. The motivation behind choosing InP-HBT's for this application can be concluded by inspecting Fig. 3 which gives the block diagram of a typical 44-GHz integrated receiver. Also illustrated is what we believe to be the preferred technology for each receiver component in terms of potential performance leverage and circuit function. At millimeter-wave frequencies, high electron mobility transistor (HEMT) technology is the undisputed choice for the low noise amplifier (LNA). However, for the high IP3 amplifier (HIA), Schottky diode mixer, local oscillator (LO) buffer amplifier, and VCO, InP-based HBT's have recently demonstrated promising performance in the millimeter-wave regime. For example, several InP-HBT VCO's have been reported at various millimeter-wave frequencies at 23.8, 40, 46, and 62 GHz and have demonstrated as much as a 23-dB improvement in phase noise over GaAs-based frequency sources [8]. It is the inherent low $1/f$ noise and high frequency characteristics of InP-HBT's which make them the preferred VCO solution at millimeter wave frequencies. InP-HBT technology has also demonstrated excellent Schottky diode mixer performance at W-band and, in fact, has been shown to require 4 dB less LO drive than an equivalent GaAs-based HEMT W-band Schottky diode design while achieving similar conversion-loss performance [9]. The low parasitic vertical MBE structure of the InP-HBT Schottky diode enables this high frequency performance, while the narrow bandgap property of the InGaAs-InP Schottky diode epitaxy material results in sub-0.4 V Schottky turn-on voltages and is responsible for its low LO power operating capability. In addition, InP-HBT's have also demonstrated high IP3 performance at millimeter-wave frequencies [5]. However, more appealing from a system standpoint is that all of these functions except the HEMT LNA can be monolithically combined on a single HBT MMIC, including the bias regulation for the HEMT LNA as recently proposed in [10]. This would enable a tremendous reduction in size, integration complexity, and cost, which has far-reaching implications in millimeter-wave phased array systems for space applications.

B. 44-GHz Amplifier Specification

Since this paper focuses on the second-stage amplifier of Fig. 3, IP3 and gain are significant parameters, whereas noise

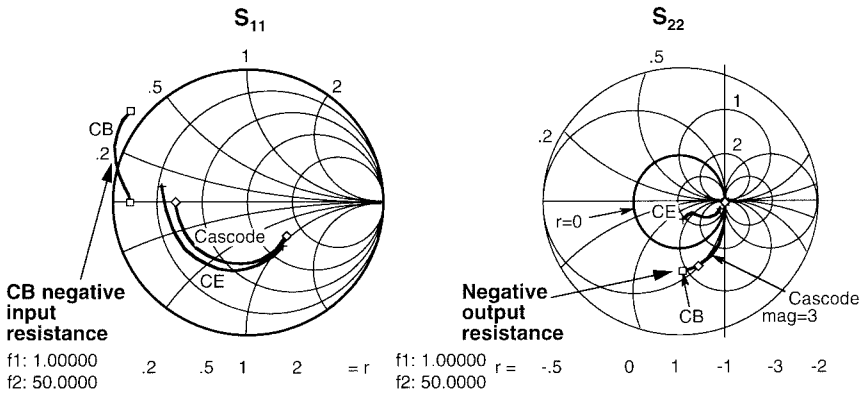


Fig. 5. Comparison of the S_{11} and S_{22} impedance characteristics of the common-emitter, common-base, and cascode device configurations.

is secondary. The goal of this design was to develop a 44-GHz amplifier with >12-dB gain and output IP3 of ≈30 dBm at 44 GHz while operating at low dc power. Also for practical implementation, monolithic self-bias using a fixed 5-V supply was highly desirable and is discussed below. In order to obtain substantial gain at 44 GHz, it was determined that a plurality of cascaded amplifier stages would be required. In order to obtain high output IP3, both the gain and the IP3 of the output stage must be high. This is indicated by the cascaded amplifier IP3 equation [11]

$$\frac{1}{\mathrm{IP}_{\mathrm{total}}} = \frac{1}{\mathrm{IP}_n} + \frac{1}{G_n \cdot \mathrm{IP}_{n-1}} + \cdots \frac{1}{G_n \cdot G_{n-1} \cdots G_k \cdots \mathrm{IP}_{k-1}} \cdots + \frac{1}{G_n \cdot G_{n-1} \cdots G_2 \cdot \mathrm{IP}_1} \quad (1)$$

where n designates the output amplifier stage, k designates an intermediate stage, a 1 designates the first amplifier stage in the chain, and where G_n and IP_n represent the gain and IP3 of the output stage, respectively. Clearly the first two terms on the right hand side of (1) dominate the expressing which determines the total IP3 of the cascaded gain chain and suggests that the output stage needs to be optimized for both high gain and IP3 simultaneously. In order to achieve maximum gain from a unit HBT cell, we choose a current density of $J_c \approx 40$ kA/cm^2, which is slightly less than the operating bias where the peak device $f_{\max}$ of ≈200 GHz is obtained. Fig. 4 compares the $G_{\max}$ of a common-emitter, a common-base, and a cascode device configuration based on a 1×10 μm^2 quad-emitter (QE) HBT unit cell (1×10 QE) with total emitter area of 40 μm^2. This figure illustrates that a common-base HBT offers a $G_{\max}$ of ≈9 dB while the cascode offers a $G_{\max}$ of ≈22 dB where the 1×10 QE devices are biased at an I_{ce} of 16 mA and a V_{ce} voltage of 2 V. This would lead us to conclude that the cascode is the best device configuration based on its available gain per unit current. However, upon careful comparison of their S_{11} and S_{22} parameters given in Fig. 5, we can observe that the common-base HBT configuration possesses a negative input impedance while both common-base and cascode device configurations possess negative output impedances. From a practical standpoint, these alternate configurations can become very unstable at millimeter-wave frequencies where device and ground via parasitics can induce potential device instability and even oscillations. Because of the attractive gain characteristics exhibited by the cascode topology, an amplifier design exercise was carried out on a "*stabilized*" cascode device cell which had resulted in higher matched gain, but relatively poorer IP3 performance compared to an equivalent common-emitter narrow-band matched design at 44 GHz. The higher gain but poorer IP3 of the cascode design are both attributed to regenerative feedback within the cascode at millimeter-wave frequencies, and therefore the cascode approach was abandoned. The common-base configuration was also abandoned because it was not amenable to the "current-sharing" bias approach and only offered a marginal improvement of 1 dB over the common-emitter configuration. For the rest of the paper we therefore assume a common-emitter configuration when referring to the HBT amplifier design.

C. Practical Bias Implementation and Optimum Bias Selection

Critical to space electronic applications is the size, weight, dc power, and cost of the RF modules and subsystem assemblies. In addition, the hardware required to provide dc voltage to the RF units such as the receivers and transmitters are very extensive, adding mass, size, dc power, and integration complexity to a system which ultimately translates into high cost. Since MMIC components optimally operate at device voltages of around 2–3 V, there is a need for custom voltage regulators and dc converters which step down the bus voltages to the appropriate device voltage, and this would be done indirectly through several tiers of regulation. However, it is more desirable to obtain MMIC's which operate from standard supplies $\geq +5$ V and which are bias-current efficient in order achieve dc power savings and eliminate the system complexity and size associated with employing additional dc regulator tiers to accommodate the lower MMIC voltage.

In order to achieve this current-efficient MMIC operation, we have adopted the current-share biasing approach shown in Fig. 6. In this approach the HBT's of different amplifier stages share the same current through a common regulated voltage supply, in this case 5 V. In this manner, the design can efficiently operate from a larger voltage supply through

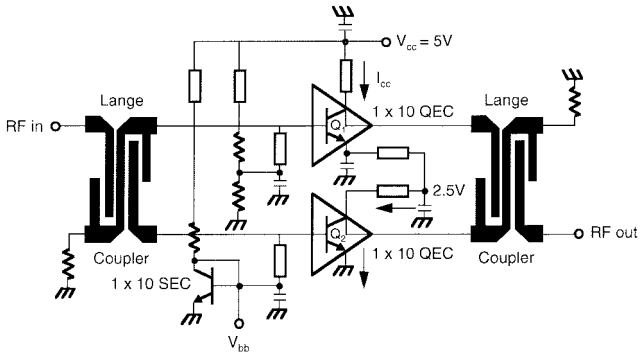


Fig. 6. Illustration of the "current-share" biasing approach as applied to a single-stage balanced amplifier.

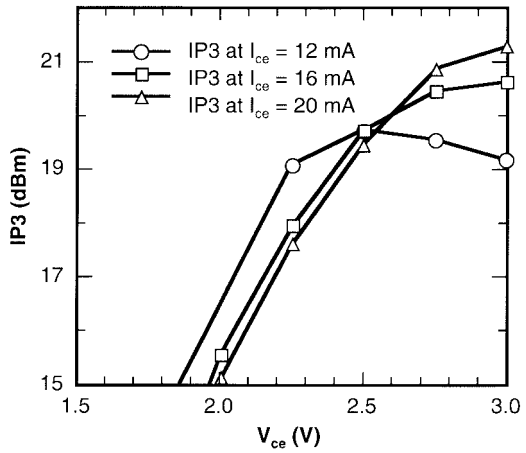


Fig. 7. IP3 at 44 GHz of a narrow-band-matched 1×10 μm^2 quad-emitter HBT device (1×10 QE) versus V_{ce} for the various I_{ce} bias currents.

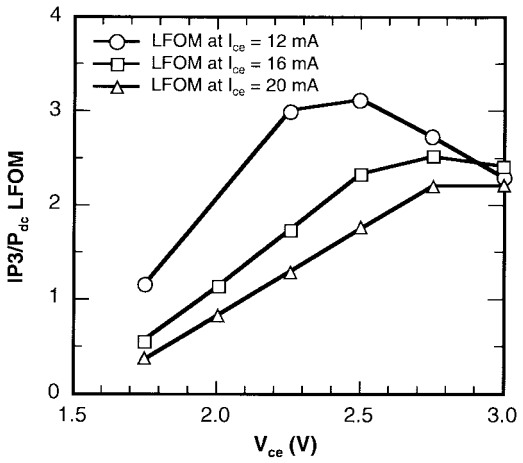


Fig. 8. IP3 per unit dc power ratio or LFOM as a function of V_{ce} voltage for the various I_{ce} bias currents.

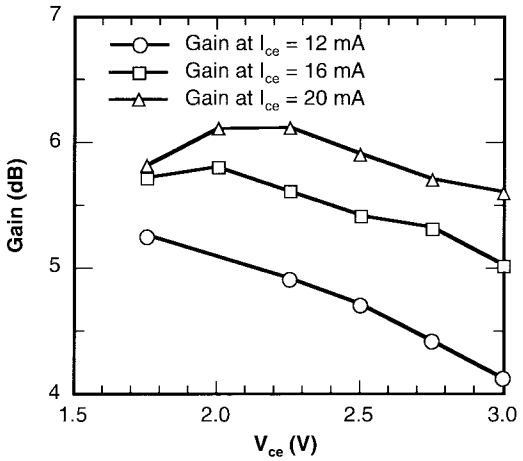


Fig. 9. Gain at 44 GHz versus V_{ce} voltage for the various I_{ce} bias currents.

reusing the bias current through multiple amplifier stages. In theory, the RF performance of each amplifier is isolated from the dc biasing components and from each other by dc bypass networks. However in practice, there is coupling between amplifiers, especially at baseband frequencies where intermodulation beat-tone products reside. Having a low-frequency active load impedance (such as the base of a common-emitter) current mirror transistor can be employed to minimize the beat-tone interaction between the amplifier stages.

From a dc viewpoint, the transistors appear as though they are cascode connected, that is, the emitter of one transistor is connected to the collector of another transistor, sharing the same bias current. From an RF standpoint, both stages appear as common-emitter amplifiers. It is obvious that the more stages that share the same supply voltage, the more efficient the MMIC dc operation. However, the supply voltage is uniformly divided between each of the transistor amplifier stages where the effective V_{ce} voltage across each HBT will decrease as the number of stages increases. This can result in a degradation in gain and IP3 performance for low V_{ce} operating voltages. Thus the performance of the HBT transistor as a function of V_{ce} must be known in order to optimize the "current-share" design approach. Fig. 7 gives the 44-GHz IP3 performance of a narrow-band-matched 1×10 μm^2 quad-emitter device (1×10 QE HBT) as a function of V_{ce} and at various I_{ce} bias currents. Fig. 8 also plots the IP3 per unit dc power ratio or "linearity figure of merit" for the various bias cases. From the plots of Figs. 7 and 8 it can be concluded that the optimum bias voltage and current which maximizes the device IP3 per unit dc power (efficiency) performance occurs at a V_{ce} of 2.5 V and an I_{ce} of 12 mA. This means that we can optimally share the current of two amplifier stages on a fixed 5-V supply where each transistor stage operates with a V_{ce} of 2.5 V. Although the IP3 per unit dc power consumption is best at this low current of 12 mA, Fig. 9 illustrates that the gain at 44 GHz is less than 5 dB, but is better with a marginal increase in bias current. As was shown from (1), the gain of the output stage is very important in determining the effective output IP3. By considering these bias-dependent gain characteristics, we arrive at the compromised bias condition of $V_{ce} = 2.5$ V and $I_{ce} = 16$ mA for the 1×10 μm^2 quad-emitter unit cell in the 44-GHz–5-V current-share amplifier application.

IV. InP-HBT IP3 Model and Load–Pull Simulations

The InP-HBT IP3 model used in the 44-GHz amplifier design of this work is based on the IP3 model developed by Maas *et al.* [12]. This model was very successful in

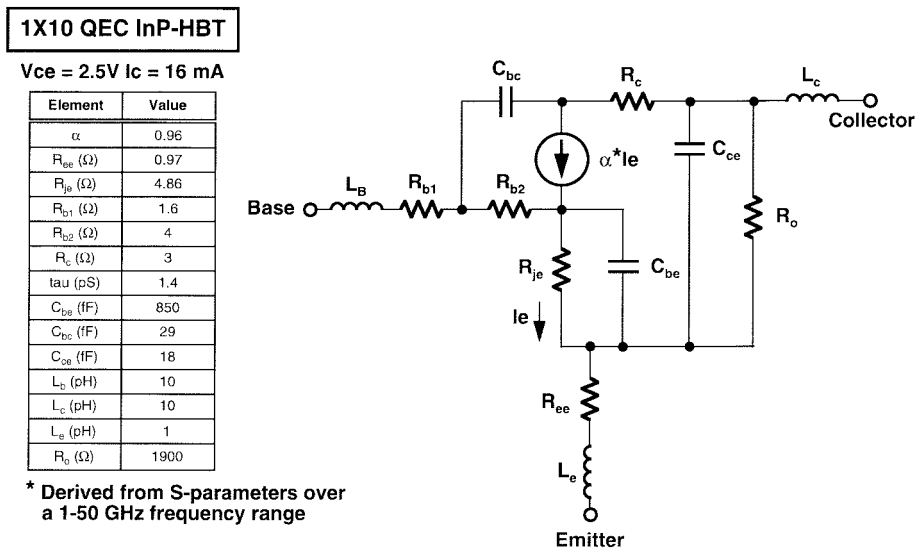
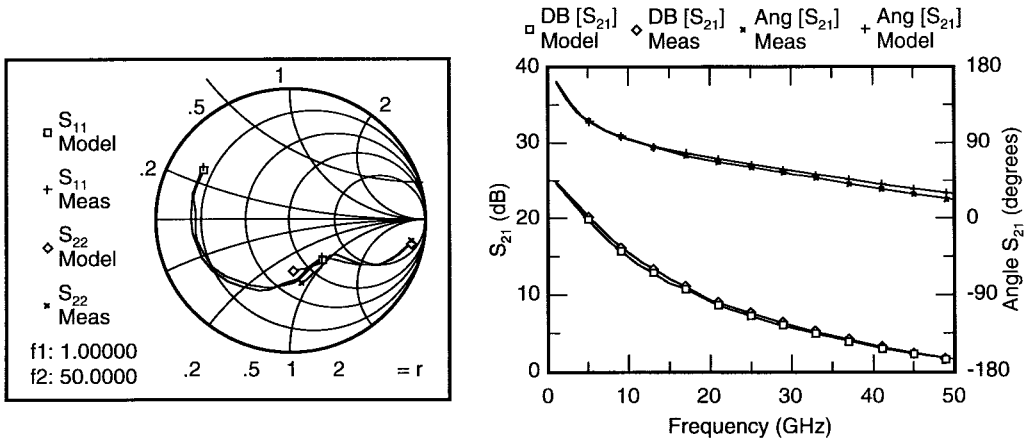


Fig. 10. The small-signal hybrid-T HBT model.



(a) (b)

Fig. 11. (a) Model fit to the measured HBT S_{11} and S_{22} characteristics and (b) model fit to the measured HBT S_{21} magnitude and angle characteristics.

predicting the gain, IP3, IP2, and IP2H performance of GaAs HBT's and amplifiers at X-band frequencies. Here, the same model and parameter extraction methodology was adopted for characterizing the InP-based HBT's, only at millimeter-wave frequencies.

The HBT IP3 model is based on the small-signal hybrid-T topology shown in Fig. 10. The small-signal model parameters were determined from a combination of both dc and s-parameter measurements. Low-frequency bias-dependent s-parameters which were later converted to z-parameters were used to extract the emitter parasitic resistance r_{ee} as described in [12]. An additional output resistance r_o has been added in order to model the finite early voltage observed in InP-HBT's (for GaAs HBT's, this parameter is set to infinity). The nominal values of the parasitic resistances R_{b1}, R_{b2}, and capacitances C_{cb}, C_{ce}, C_{be} were determined through a combination of dc measurements and physical calculations. The model was then optimized over a 1–50 GHz frequency range using reasonably constrained parameters. The left-hand-side table shown in Fig. 10 gives the resultant optimized small-signal parameters of a 1×10 μm^2 quad-emitter HBT unit cell for the previously determined bias condition of $V_{ce} = 2.5$ V and $I_{ce} = 16$ mA. Fig. 11(a) illustrates the model fit to the measured HBT S_{11} and S_{22} characteristics, while Fig. 11(b) illustrates the model fit to the measured HBT S_{21} magnitude and angle characteristics. These figures show excellent agreement between device model and the small-signal s-parameter characteristics over a 1–50 GHz frequency range.

The complete nonlinear HBT model is given in Fig. 12. This HBT model includes the nonlinear dynamic resistance (nonlinear G_m) of the exponential base-emitter junction, a nonlinear base-emitter diffusion capacitance C_{be}, and a nonlinear current source $Ic(I_e)$ as outlined in [12]. Each of these nonlinearities are expressed as third-order polynomials as illustrated in Fig. 12 and describe their weakly nonlinear characteristics as discussed in great detail in [12]. The first coefficients in each equation g_1, α_1, and c_1, are fundamental linear coefficients which describe the device transconductance $g_m = (q \cdot Ic)/(nKT)$, the emitter to collector current gain $\alpha = (\beta/1 + \beta)$, and the base-emitter diffusion capacitance

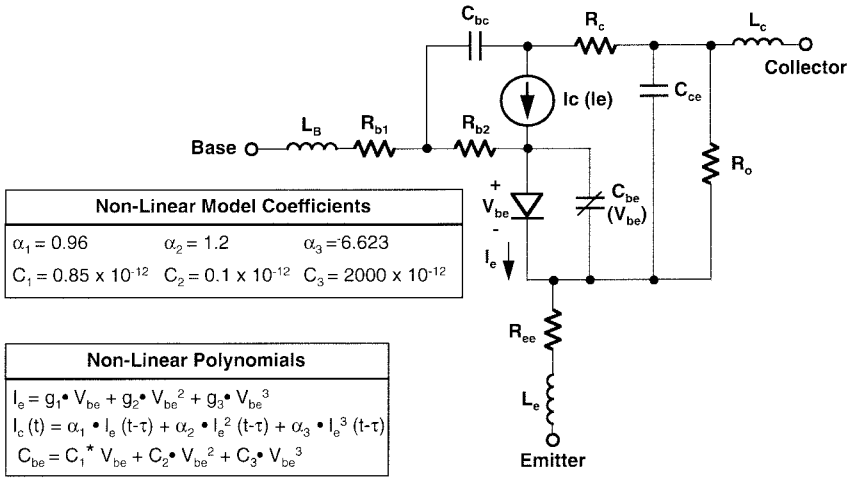


Fig. 12. The complete HBT IP3 model including the nonlinear elements, $I_e(V_{be})$, $I_c(I_e)$, and $C_{be}(V_{be})$.

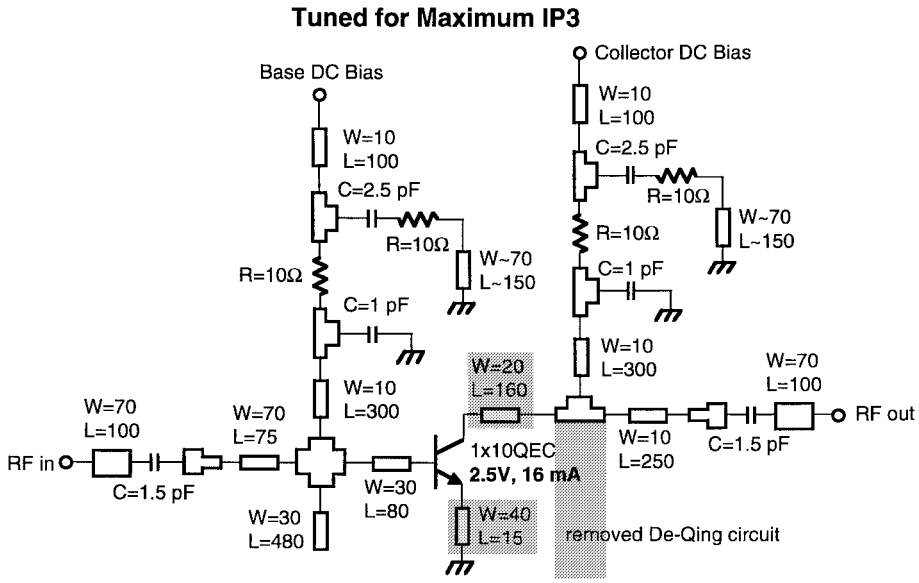


Fig. 13. Detailed circuit schematic reflecting the modifications to the prematched HBT device output network as a result of simulated IP3 load tuning.

$C_{be} = \tau \cdot g_m$, respectively. Coefficients g_2 and g_3 can also be calculated while the second and third coefficients of the I_c and C_{be} polynomials which heavily determine the second- and third-order intermodulation characteristics of the HBT can be found empirically by adjusting the coefficients to match the measured second harmonic and third-order intercept points of the HBT. In particular, the second-order coefficients are adjusted to match the second harmonic characteristics while the third-order coefficients are adjusted to match the third-order characteristics of the HBT. This exercise was performed on a 1×10 μm^2 quad-emitter HBT unit cell (1×10 QE) device over a broad frequency range from 30–50 GHz. The resulting coefficients are given in the table of Fig. 12. The parameter c_3 was adjusted for a "best fit" to measured device IP3 across this broad band. However, the c_3 coefficient was then readjusted to match the measured IP3 characteristics of a 44-GHz conjugately matched 1×10 QE HBT in order to offer a more accurate IP3 fit at the 44-GHz design frequency. A value of 600×10^{-12} pF/V^3 for coefficient c_3 was determined to produced the best IP3 fit at 44 GHz. The measured and modeled value of IP3 at 44 GHz for the conjugate matched 1×10 QE HBT is 19.5 dBm.

Since the model now accurately matches the measured IP3 of the conjugate matched 1×10 QE HBT at 44 GHz, the output network was modified and tuned to obtain the best combination of IP3 and gain using harmonic balance simulations. Fig. 13 gives a detailed schematic of the resulting "IP3-tuned" 1×10 QE HBT prematched structure. This topology consists of simple series-shunt microstrip matching networks for the conjugate-matched input and "IP3-tuned" output. Compared to the original conjugate-matched output network, a de-Qing network was removed as well as an adjustment in the length of a microstrip line directly connected to the device collector. It was also found that IP3 and gain were both sensitive to the series feedback transmission line connected to the emitter. By reducing the length of this microstrip line, higher gain was achieved at little expense to the IP3 and stability performance. Although these design

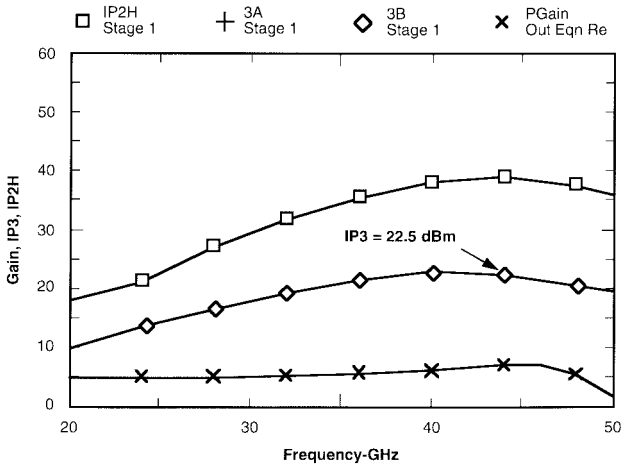


Fig. 14. Simulations indicating a 3 dB improvement in IP3 performance of the prematched HBT amplifier. The resultant IP3 is now 22.5 dBm at 44 GHz.

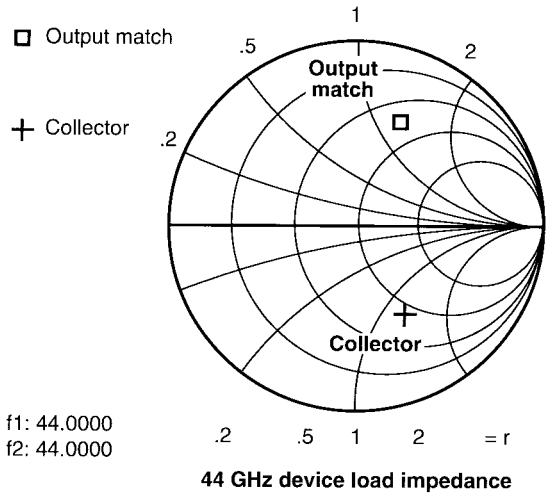


Fig. 15. Simulated output impedance match looking out from the collector, as well as the impedance looking into the collector.

changes appear minor, it had a great impact on the IP3 performance of the amplifier. As indicated in Fig. 14, the IP3 is now 22.5 dBm at 44 GHz as a result of the new output match which is a 3 dB improvement over the original conjugate-matched design. Fig. 15 gives the resultant output impedance match looking out from the collector, as well as the impedance looking into the collector. The optimum IP3 match appears to be very close to the conjugate match of the collector and is not greatly different; however, the output matching network configuration which was used to achieve these characteristics is significantly different. This suggest that the matching impedance at the beat-tone or other frequencies may play a significant role in the amplifier IP3. Nevertheless, as will be confirmed later, a significant improvement in amplifier IP3 was obtained by load tuning the output match based on this IP3 model and load–pull simulations.

V. 44-GHz High Intercept Amplifier

The 44-GHz IP3-matched HBT device described above was used to construct the Q-band high intercept amplifier of this paper. Fig. 16 shows a detailed schematic of the single-stage "double balanced" amplifier which incorporates current reuse biasing. This topology employs four Lange couplers to construct two identical single-balanced amplifiers which are subsequently combined into a double-balanced amplifier using two more Lange couplers. In this manner, four of the prematched HBT devices described in the previous section are combined in order to obtain an approximate 6 dB increase in IP3. Bias current is shared between the adjacent prematched 1×10 μm$^2\times$ four-emitter-finger (1×10 QEC) HBT. This reduces the overall amplifier current consumption by $\approx$40% for a standard 5-V supply. The 10% loss is due to the nonreusable current mirror bias of the 1×10 SE HBT transistor. However, this could be reduced to less than a 2% loss if the area of the current mirror HBT transistor is reduced by a factor of five. The current sharing between adjacent matched transistor cells is done by a totem pole connection where the emitter of the top cell is fed to the collector of the bottom cell. A bypass capacitor on the emitter of the top cell is used to provide an RF-ground for common-emitter operation. It should be noted that the value of this capacitor must be chosen very carefully in order to maintain the stability performance of the amplifier. This is a nontrivial point and should be carefully investigated. As shown in Fig. 17, a shunt damping resistor r_{stb} incorporated in the schematic of Fig. 16 was found to help the out-of-band stability performance in the simulations, but was not required. From this figure it can be concluded that an r_{stb} of $\approx 5\ \Omega$ would ensure unconditionally stable amplifier operation.

The V_{cc} potential of 5 V was equally split across adjacent 1×10 QEC HBT prematched device cells which have V_{ce}'s of 2.5 V each. The current share approach was found to be well suited with the double-balanced amplifier topology which integrates the four prematched HBT cells using the six Lange couplers. The Lange coupler two-way combining approach has the benefits of increasing the IP3 by $\approx$3 dB while preserving the gain and bandwidth performance of the single-ended amplifier design blocks. In our design it was found that the IP3 increased by 3.5 dB by balancing two prematched stages while the overall combined gain incurred only a 0.3–0.4 dB Lange coupler combining loss. The more than 3 dB improvement might be explained by the resistive 50 Ω terminations which absorb the reflections due to poor out-of-band voltage standing wave ratio (VSWR) mismatch. By further combining two of these balanced stages, we end up with a four-way combiner topology with another 3 dB increase in IP3. While the addition of another Lange combining stage decreased the gain of the overall amplifier by another 0.3–0.4 dB, clearly this approach benefits in overall IP3 performance.

The Lange coupler balanced design not only enables high IP3-bandwidth performance, but also provides excellent out-of-band return-loss performance which improves its practical insertability with mixer components. Because of its excellent input and output return-loss, three stages of these double-balanced amplifiers were cascaded with negligible gain degradation.

Fig. 18 gives the block diagram and gain-IP3 budget of the resultant three-stage double-balanced InP-HBT amplifier.

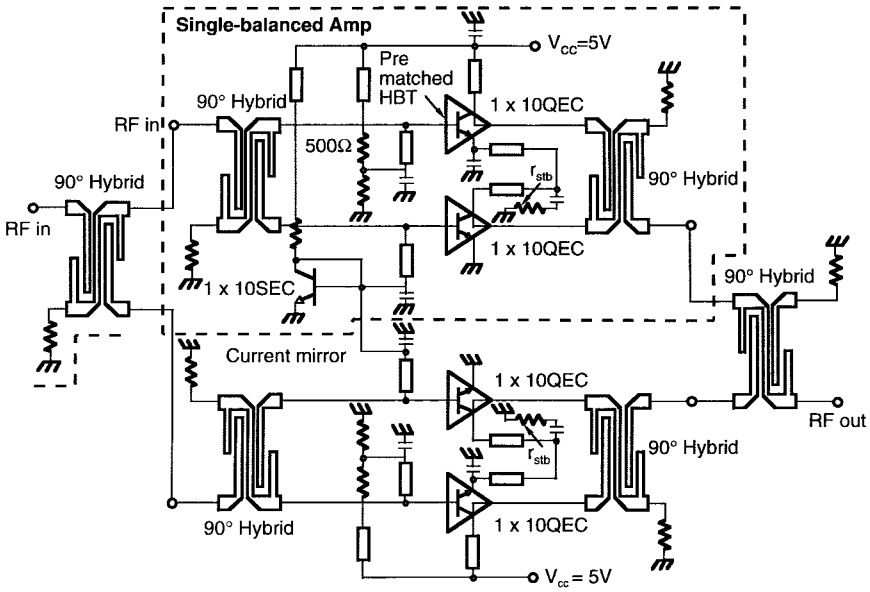


Fig. 16. Detailed schematic of the single-stage double balanced amplifier with current reuse biasing.

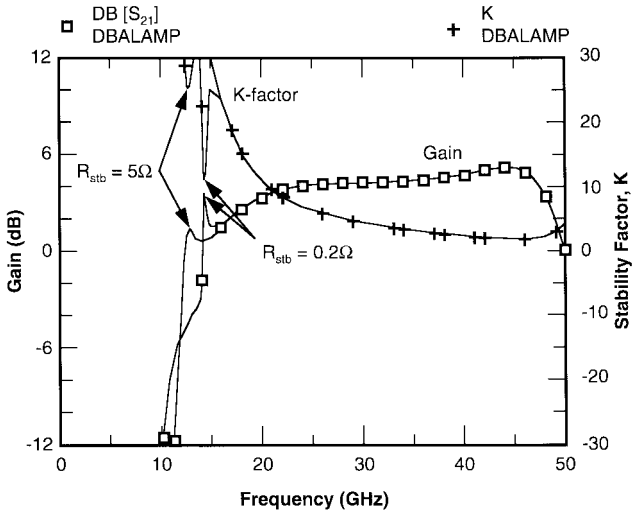
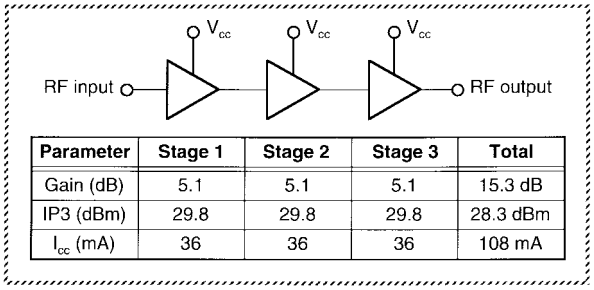


Fig. 17. Simulated stability performance ("k-factor") and the effects of using a damping resistor r_{stb} of $\approx 5\ \Omega$. The addition of this stability resistor ensures unconditionally stable amplifier operation.



Parameter	Stage 1	Stage 2	Stage 3	Total
Gain (dB)	5.1	5.1	5.1	15.3 dB
IP3 (dBm)	29.8	29.8	29.8	28.3 dBm
I_{cc} (mA)	36	36	36	108 mA

Fig. 18. Block diagram and gain-IP3 budget of the three-stage double-balanced InP-HBT amplifier.

Three stages were chosen in order to provide a practical gain of 15.3 dB at 44 GHz. Because of the low gain per stage of ≈5.1 dB, the first two stages must have a relatively high IP3 with respect to the output stage in order to minimize IP3 degradation through the amplifier chain in accordance with the cascaded IP3 (1). In this design the first and second stages are identical to the high IP3 output stage in order to obtain a cumulative IP3 of 28.3 dBm. As a consequence, the overall IP3 is only degraded by 1.5 dB by cascading the three stages. It should be noted that cascode stages were considered for obtaining more gain per stage, however, simulations indicated that this configuration is detrimental to IP3, as discussed in Section III, and also would have precluded the use of the current share bias approach in a fixed 5-V system.

Fig. 19 shows a microphotograph of the resultant three-stage double-balanced amplifier MMIC. The InP-HBT MMIC chip fits into a compact 6.2 × 3.5 mm^2 area, integrates 15 HBT's and 18 Lange couplers, and represents one of the highest complexity InP-HBT MMIC's demonstrated at millimeter-wave frequencies. Furthermore, the MMIC employs a fully self-biased current-share approach which enables it to operate efficiently from a single 5-V supply.

VI. Measured Results

Fig. 20 gives the measured gain and return-loss performance. The simulated gain is also shown for comparison. A gain of 15.4 dB is achieved at 44 GHz with input and output return-losses better than −15 dB across a 25–50 GHz band. The excellent return-loss is due to the use of the balanced Lange coupler amplifier topology. The simulated gain matches the data to within 1 dB at 44 GHz, however, the simulation is more optimistic at lower frequencies. This is believed to be due to the proximity effects of the layout which was not simulated using electromagnetic simulation tools.

Fig. 21 gives the measured versus simulated three-stage amplifier IP3 under the nominal design bias condition. The measured IP3's are 28.3 and 28.8 dBm at 44 and 46 GHz, respectively. At 44 GHz, the calculated IP3/$P_{\rm dc}$ linearity figure-of-merit for the output stage is 5.3 : 1 and is believed to be the highest reported for an InP-based HBT amplifier in

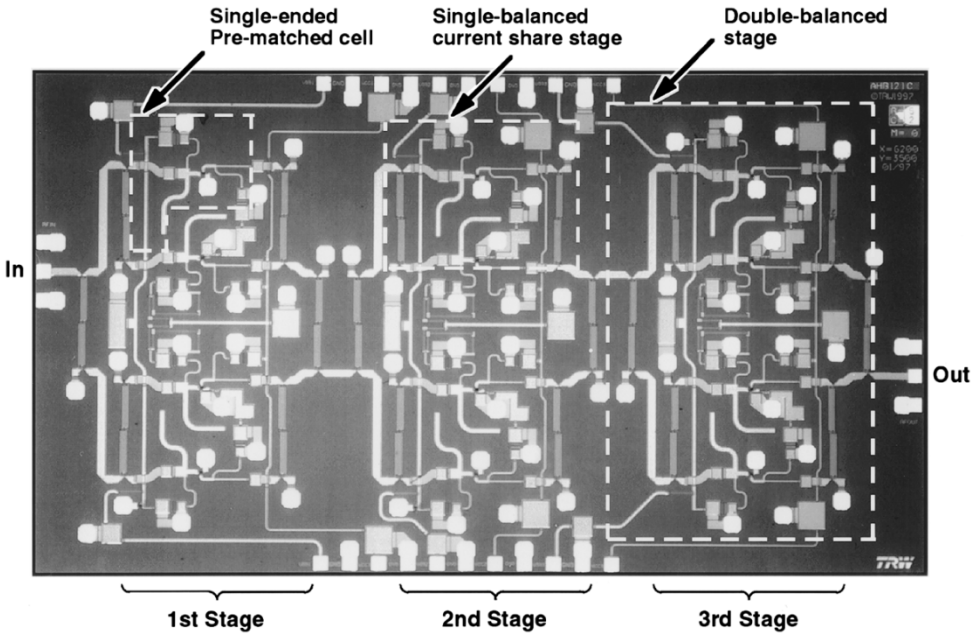


Fig. 19. Microphotograph of the three-stage double-balanced amplifier MMIC. The InP-HBT MMIC chip fits into a compact 6.2 × 3.5 mm^2 area.

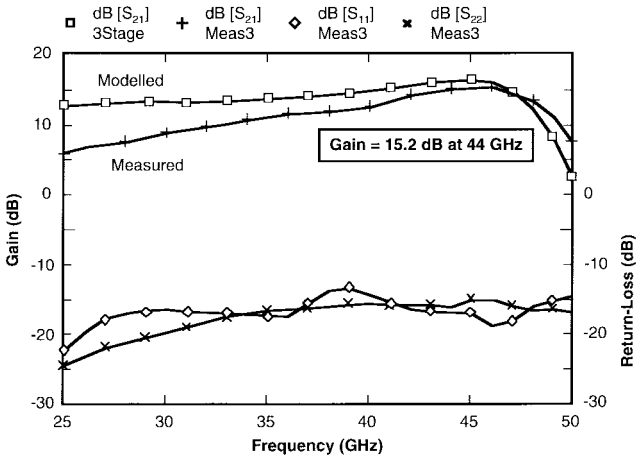


Fig. 20. Measured gain and return-loss performance of the three-stage InP-HBT amplifier. The simulated gain is also shown for comparison.

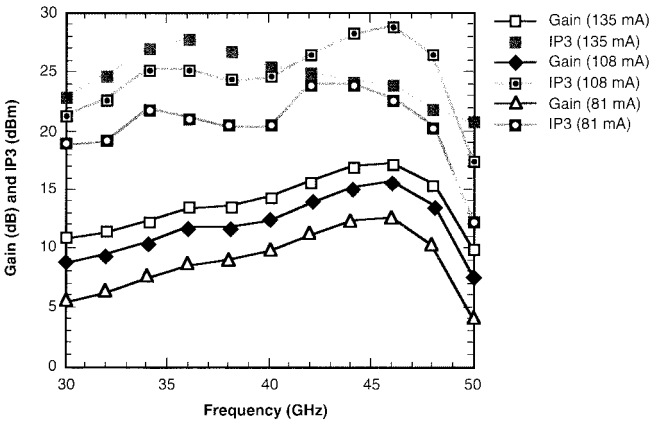


Fig. 22. Measured IP3 and gain at low, medium, and high bias current. Optimum IP3 performance occurs at the nominal design current of 108 mA due to the optimal IP3 matching conditions.

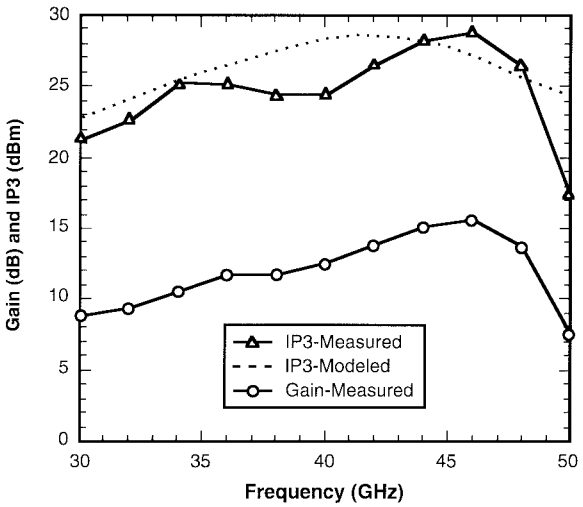


Fig. 21. Measured versus simulated amplifier IP3 performance under the nominal design bias.

the 44-GHz frequency regime. This number is calculated from the single stage IP3 of 29.8 dBm which is the extracted output stage IP3 given in the gain-IP3 chain analysis of Fig. 18. Note that the IP3 matches reasonably well across a 35–48 GHz band with the exception of a dip in the measured IP3 at around 40 GHz. This correlates to a dip in the gain response which was also evident in the scattering parameter measurements. This dip is believed to be caused by internal RF coupling between the current shared prematched stages; however, this discrepancy occurs in a region outside of the 44-GHz band of interest. At the 44-GHz frequency of interest, however, the IP3 matches to within 1 dB. This not only validates our IP3 model, but also validates the 3 dB design improvements obtained from the IP3 load–pull simulations based on the model. Fig. 22 also gives the measured IP3 and gain at low, medium, and high bias current. It is shown that as the current is increased from 81 to 135 mA through the MMIC, the gain improves by as much as 5 dB. However, IP3 appears to be optimal at the nominal

design current of 108 mA and is probably due to the optimal IP3 matching conditions at this bias level. At this bias, the measured saturated output power P_{sat} is 16.2 dBm.

VII. Conclusion

The high IP3 performance and practical bias capability of an InP-HBT-based 44-GHz amplifier was demonstrated. A single-stage IP3/$P_{\rm dc}$ ratio of 5.3 : 1 was achieved at 44 GHz and is believed to be among the highest reported for an InP HBT amplifier at this frequency. An HBT IP3 model and load–pull simulations were used in designing a 3-dB improvement in IP3 of the prematched cell. In addition, a practical current share bias approach was employed with the double-balanced HBT amplifier design topology which resulted in a 40% reduction in current consumption through a standard 5-V supply. The high IP3, millimeter-wave frequency, and low voltage performance of InP HBT's make them attractive for commercial digital radio receiver applications.

Acknowledgment

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